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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,053	01/18/2002	Santosh C. Lolayekar	E003 - 1008US0	1750

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EXAMINER	
REILLY, SEAN M	
ART UNIT	**PAPER NUMBER**
2153	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,053	LOLAYEKAR ET AL.	
	Examiner	Art Unit	
	Sean Reilly	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This application has been assigned to another Examiner.

This action is in response to Applicant's amendment and request for reconsideration filed on November 7, 2005. Claims 1-6 and 8-26 are presented for further examination. All independent claims except claim 11 have been amended. This action is made NON-FINAL since a new grounds of rejection is set forth with regard to claim 11. Note the previous Examiner did not reject claim 11 under 35 U.S.C. 102 or 103 in the last action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 3, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Molero et al. ("On the Switch Architecture for Fibre Channel Storage Area Networks," June 2001, hereinafter "Molero") and Epps et al. (U.S. Patent Number 6,295,575; hereinafter Epps).

In considering claim 1, Molero discloses a method for use in a system for storing and accessing data ("SAN"), the system including at least one initiator ("source") and at least one target comprising a mirrored virtual target or a physical storage device ("destination," which is a storage device – i.e. "disk" – in the Molero system) and at least one switch ("switch"), the initiator, target, and switch communicating using at least one network ("SAN"), the at least one

switch including a plurality of ports ("ports") and a processing unit (inherent for the switch processing), wherein the processing unit is associated with at least one port of said plurality of ports to provide load balancing at said at least one port ("destination disk of each I/O operation initiated by a server is randomly chosen among all the disks in the network," § 3.2), the method comprising:

Providing a plurality of request paths over the network to the target from switch, each path passing through at least one port of the switch ("selecting an output link," wherein an "output port" is used to connect to one of the target disks over the network as shown in Fig. 2 and described on p. 486);

Receiving at said at least one port, a plurality of storage input/output requests (§ 3.2 describes that I/O requests between a server initiator and a storage device target pass through the switch); and

For each request at said one or more ports, dynamically load balancing each request among the paths by using said processing unit associated with said one or more ports to determine an appropriate path by using the processing unit associated with said one or more ports to determine the appropriate path ("destination disk of each I/O operation initiated by a server is randomly chosen among all the disks in the network," § 3.2).

Molero disclosed the invention substantially as claimed however Molero failed to specifically recite using a plurality of processing units wherein each processing unit is associated with at least one port of said plurality of ports to provide load balancing at said port. Nonetheless such processing was widely known in the art at the time of the invention, as evidenced by Epps. In an analogous art, Epps disclosed a switching system that utilizes a line

card pipelining scheme to service requests that arrive at switch ports (abstract). Epps's system has a plurality of line cards that each process incoming requests across switch ports associated with that line card (Col 4, line 60 – Col 5, line 2). Each line card contains its own processing pipeline along with a CPU for processing the incoming packets at each port (Figure 2, CPU 1240). Therefore a switch contains a plurality of processing units (CPUs) since a switch contains multiple line cards and each line card contains a CPU. In Epps's system the CPU on each line card dynamically load balances each request at the port (see inter alia during TLU look-up, Col 6, lines 40-46, load balancing is preformed Col 23, lines 16-37). Epps's further disclosed that the disclosed pipelining line card configuration reduces latency and operates as close to line rate as possible i.e. at or near the maximum speed of transmission over the physical medium and without any appreciable buffering delay. Thus, it would have been obvious to one of ordinary skill in the art to incorporate the switch line card pipelining scheme disclosed by Epps within Molero's system in order to reduce latency and operate as close to line rate as possible i.e. at or near the maximum speed of transmission over the physical medium and without any appreciable buffering delay.

In considering claim 3, Molero further discloses that the target is a physical storage device ("storage device," see § 1).

In considering claim 4, Molero further discloses that the target is a virtual target (the software receiving the communication at the storage device is a "virtual" target).

2. **Claims 2, 5, 6, 8-10, and 15-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Molero and Epps, in view of Jindal et al. (U.S. Patent No. 6,324,580, hereinafter "Jindal"), and further in view of Ito et al. (U.S. Patent No. 5,721,904, hereinafter "Ito").**

In considering claim 2, the system taught by Molero discloses dynamically load balancing to select the paths, but does not describe that the load balancing is based on a path having the shortest average response time (instead, Molero describes distributing the load via a "random" scheme – see § 3.2). Nonetheless, in a similar art, Jindal discloses a load balancing method for balancing load among mirrored target storage systems ("servers"), including determining a response time for each path, and passing a request received by the load balancer from an initiator to a target along the path with the shortest response time (col. 5, lines 26-63; col. 6, lines 37-40, "the selected policy requires choosing the least-loaded server (e.g., that which has the fastest response time)"). Given the teaching of Jindal, a person having ordinary skill in the art would have readily recognized the desirability and advantages of including the load balancing scheme taught by Jindal in the system taught by Molero, because using the path with the shortest response time will ensure a faster response and reduce the delay for requests. Thus, it would have been obvious to use the shortest response time load balancing method taught by Jindal to balance the load between the target storage disks in the system taught by Molero.

Note that the combined system of Jindal and Molero does not disclose measuring a shortest *average* response time, as claimed. Nonetheless, using a shortest average response time to determine which target to select in a load balancing system is well known, as evidenced by Ito (col. 18, lines 30-36, "the selection operation by one or both of the methods based on response

time is executed a plurality of times [so] that the server component having the shortest average response time is selected"). Given this teaching, it would have been obvious to a person having ordinary skill in the art to load balance in the system taught by Jindal and Molero according to a shortest *average* response time, as taught by Ito, to "[prevent] the effect of change in temporary network traffic congestion" (see Ito, col. 18, lines 34-36).

In considering claim 5, claim 5 includes the same limitation as claim 2, and adds that the target is a mirrored target with a plurality of members. Molero further discloses that the target is a mirrored target with a plurality of members (i.e. one of four disks - § 3.1).

In considering claim 6, Molero further discloses that the request can be a read request ("read operations," § 3.2, ¶ 1).

In considering claim 8, claim 8 contains no further limitations over claims 1 and 2 combined, except that the target is a storage device. Nonetheless, the array of mirrored disks taught by Molero can be considered a storage device. Thus, claim 8 is rejected for the same reasons as claims 1 and 2 combined.

In considering claim 9, claim 9 contains no further limitations over claims 1 and 2 combined, except that the target is a mirrored virtual target having a plurality of members. Nonetheless, the array of mirrored disks taught by Molero constitutes a mirrored virtual target

having a plurality of members. Thus, claim 8 is rejected for the same reasons as claims 1 and 2 combined.

In considering claim 10, Molero further discloses that the request can be a read request ("read operations," § 3.2, ¶ 1).

In considering claim 15, describes a switch that includes similar limitations as claims 1 and 2 combined. Therefore, claim 15 is rejected for the same reasons as claims 1 and 2 combined.

In considering claim 16, the load balancing circuitry will necessarily include a storage processor and CPU.

In considering claim 17, claim 17 contains no further limitations over claim 15 and is rejected for the same reason.

In considering claim 18, Jindal further discloses means for maintaining statistics for the response time of each path (col. 6, lines 15-18, "collect, assemble and analyze the various pieces information") and means for passing a request received by the switch from the initiator to the target along the path with the shortest response time ((col. 5, lines 26-63; col. 6, lines 47-40, "the selected policy requires choosing the least-loaded server (e.g., that which has the fastest response time)")

Note that the combined system of Jindal and Molero, as described earlier, does not disclose measuring a shortest *average* response time, as claimed. Nonetheless, using a shortest average response time to determine which server to select in a load balancing system is well known, as evidenced by Ito (col. 18, lines 30-36, "the selection operation by one or both of the methods based on response time is executed a plurality of times [so] that the server component having the shortest average response time is selected"). Given this teaching, it would have been obvious to a person having ordinary skill in the art to load balance in the system taught by Jindal and Molero according to a shortest *average* response time, as taught by Ito, to "[prevent] the effect of change in temporary network traffic congestion" (see Ito, col. 18, lines 34-36).

In considering claim 19, claim 19 describes a storage network that includes the no further substantive features over the features described in claims 1 and 2 combined, and is thus rejected for the same reasons.

In considering claim 20, Molero further discloses that the target is a physical storage device ("storage device," see § 1).

In considering claim 21, Molero further discloses that the target is a virtual target (the software receiving the communication at the storage device is a "virtual" target).

In considering claim 22, Molero further discloses that the target is a mirrored target with a plurality of members ("disks") wherein the plurality of paths are respective paths to each member (i.e. each member is connected to a different port of the switch).

In considering claim 23, claim 23 describes a machine readable media for performing the same functions as claims 1 and 2 combined, and is thus rejected for the same reasons.

In considering claim 24, Molero further discloses that the target is a physical storage device ("storage device," see § 1).

In considering claim 25, Molero further discloses that the target is a virtual target (the software receiving the communication at the storage device is a "virtual" target).

In considering claim 26, claim 26 presents the same substantive steps as claim 2, and is thus rejected for the same reasons as discussed with regard to claims 1 and 2.

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Molero, in view Jindal and further in view of Ito.

In considering claim 11, claim 11 presents the same limitations as claim 8 without the requirement for a plurality of processing units, and further describes that selection method applies to two separate initiators making requests to both physical storage devices and mirrored

targets with a plurality of members. Nonetheless, as described with regard to claims 8 and 9, Bhaskaran discloses that the targets are both physical storage devices (i.e. servers) and mirrored targets with a plurality of members (col. 1, lines 34-46, describing a "cluster" of servers with the same "virtual" IP address that can all respond to requests for particular information).

4. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Molero and Jindal and Ito and further in view of Epps.

Molero disclosed the invention substantially as claimed however Molero failed to specifically recite using line cards for processing requests. Nonetheless the use of line cards was widely known in the art at the time of the invention, as evidenced by Epps. In an analogous art, Epps disclosed a switching system that utilizes a line card pipelining scheme to service request that arrive at switch ports (abstract). Epps's system has a plurality of line cards that each process incoming requests across switch ports associated with that line card (Col 4, line 60 – Col 5, line 2). Each line card contains its own processing pipeline along with a CPU for processing the incoming packets at each port (Figure 2, CPU 1240). Therefore a switch contains a plurality of processing units (CPUs) since a switch contains multiple line cards and each line card contains a CPU. In Epps's system the CPU on each line card dynamically load balances each request at the port (see inter alia during TLU look-up, Col 6, lines 40-46, load balancing is preformed Col 23, lines 16-37). Epps's further disclosed that the disclosed pipelining line card configuration reduces latency and operates as close to line rate as possible i.e. at or near the maximum speed of transmission over the physical medium and without any appreciable buffering delay. Thus, it would have been obvious to one of ordinary skill in the art to

incorporate the switch line card pipelining scheme disclosed by Epps within Molero's system in order to reduce latency and operate as close to line rate as possible i.e. at or near the maximum speed of transmission over the physical medium and without any appreciable buffering delay.

Response to Arguments

Applicant's arguments are moot in view of the new grounds of rejection set forth.

Conclusion

The prior art made of record, in PTO-892 form, and not relied upon is considered pertinent to applicant's disclosure.

This office action is made **NON-FINAL.**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean Reilly whose telephone number is 571-272-4228. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glen Burgess can be reached on 571-272-3949. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 6, 2006

KRISNA LIM
PRIMARY EXAMINER